

## Claims

- 1) Method for regulating a jitter buffer (JP) for buffering a data packet stream wherein
  - 5 a) a transmission delay ( $d_p$ ) due to buffering is in each case registered for the data packets (DP1, DP2, DP3) of the data packet stream,
  - b) weighted mean delay values ( $d_1$ ) are continuously derived from registered transmission delays ( $d_p$ ), with a shorter transmission  
10 delay being weighted higher than a longer transmission delay, and
  - c) a read-out speed (CLK) of the jitter buffer (JP) is regulated as a function of the continuously derived weighted mean delay values ( $d_1$ ) in such a way that said values are adjusted as a regulating variable to a predefined desired delay ( $sd_1$ ).
- 15 2) Method according to Claim 1 characterized in that a new weighted mean delay value ( $d_1$ ) is derived from a previously derived weighted mean delay value and a currently registered  
20 transmission delay ( $d_p$ ).
- 3) Method according to one of the preceding Claims characterized in that a currently registered transmission delay ( $d_p$ ) is compared with a  
25 previously derived weighted mean delay value, and the weighting of the currently registered transmission delay ( $d_p$ ) is determined as a function of the result of the comparison.
- 4) Method according to Claim 3  
30 characterized in that the currently registered transmission delay ( $d_p$ ) is weighted with a first predefined weight value ( $\beta_1$ ) if the currently registered transmission delay ( $d_p$ ) is shorter than the previously derived weighted mean delay value and is weighted with a second predefined  
35 weight value ( $\beta_2$ ) if the currently registered transmission delay ( $d_p$ ) is longer than the previously derived weighted mean delay value, with the first weight value ( $\beta_1$ ) being larger than the second weight value ( $\beta_2$ ).

- 5) Method according to one of the preceding Claims characterized in that the regulating variable ( $d_1$ ) is regulated by a single regulating circuit.

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- 6) Jitter buffer regulating circuit for regulating a jitter buffer (JP) for buffering a data packet stream with

a) a registration device (EE) for registering a transmission delay ( $d_p$ ) due to buffering of a respective data packet (DP1, DP2, DP3) of the data packet stream,

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a) a mean-forming device (ME) for continuously deriving weighted mean delay values ( $d_1$ ) from registered transmission delays ( $d_p$ ), with higher weighting of a shorter transmission delay compared to a higher transmission delay, and

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b) a regulating device (RE) for adjusting the continuously derived weighted mean delay values ( $d_1$ ) to a predefined desired delay ( $sd_1$ ) by means of regulating a read-out speed (CLK) of the jitter buffer (JP) as a function of the continuously derived weighted mean delay values ( $d_1$ ).

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